IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 10/108,972, filed March 28, 2002, ~~pending~~ now U.S. Patent 6,632,732, issued October 14, 2003, which is a divisional of application Serial No. 09/843,118, filed April 26, 2001, now U.S. Patent 6,468,891, issued October 22, 2002, which is a divisional of application Serial No. 09/511,986, filed February 24, 2000, pending.

Please replace paragraph number **[0009]** with the following rewritten paragraph:

[0009] Typically, reinforced polymeric materials are employed as the dielectric substrates of rigid circuit boards. The most commonly used dielectric substrate material is ~~glass-reinforced~~ glass-reinforced epoxy. Some circuit boards are made from polyimide resins so as to withstand higher temperatures. Other dielectric materials have also been developed and used to fabricate the dielectric substrates of circuit boards.

Please replace paragraph number **[0021]** with the following rewritten paragraph:

[0021] The mathematical simulation or model is then employed to generate an actual object by building the object, layer by superimposed layer. A wide variety of approaches to stereolithography by different companies has resulted in techniques for fabrication of objects from both metallic and nonmetallic materials. Regardless of the material employed to fabricate an object, stereolithographic techniques usually involve disposition of a layer of unconsolidated or unfixed material corresponding to each layer within the object boundaries, followed by selective consolidation or fixation of the material to at least a partially consolidated, or ~~semi-solid,~~ semi-solid state in those areas of a given layer corresponding to portions of the object, the consolidated or fixed material also at that time being substantially concurrently bonded to a lower layer of the object being fabricated. The unconsolidated material employed to build an object may be supplied in particulate or liquid form, and the material itself may be consolidated or fixed, or a separate binder material may be employed to bond material particles to one another

and to those of a ~~previously formed~~ previously formed layer. In some instances, thin sheets of material may be superimposed to build an object, each sheet being fixed to a next lower sheet and unwanted portions of each sheet removed, a stack of such sheets defining the completed object. When particulate materials are employed, resolution of object surfaces is highly dependent upon particle size, whereas when a liquid is employed, surface resolution is highly dependent upon the minimum surface area of the liquid which can be fixed and the minimum thickness of a layer that can be generated. Of course, in either case, resolution and accuracy of object reproduction from the CAD file is also dependent upon the ability of the apparatus used to fix the material to precisely track the mathematical instructions indicating solid areas and boundaries for each layer of material. Toward that end, and depending upon the layer being fixed, various fixation approaches have been employed, including particle bombardment (electron beams), disposing a binder or other fixative (such as by ink-jet printing techniques), or irradiation using heat or specific wavelength ranges.

Please replace paragraph number **[0058]** with the following rewritten paragraph:

[0058] Before fabrication of a first layer for a support 122 or an object to be fabricated is commenced, the operational parameters for apparatus 80 are set to adjust the size (diameter if circular) of the laser light beam used to cure material 86. In addition, computer 82 automatically checks and, if necessary, adjusts by means known in the art the surface level 88 of material 86 in reservoir 84 to maintain same at an appropriate focal length for laser beam 98. U.S. Patent No. 5,174,931, referenced above and previously incorporated herein by reference, discloses one suitable level control system. Alternatively, the height of mirror 94 may be adjusted responsive to a detected surface level 88 to cause the focal point of laser beam 98 to be located precisely at the surface level 88 of material 86 ~~at surface level 88~~ if the surface level 88 is permitted to vary, although this approach is more complex. Platform 90 may then be submerged in material 86 in reservoir 84 to a depth equal to the thickness of one layer or slice of the object to be formed, and the liquid surface level 88 is readjusted as required to accommodate material 86 displaced by submergence of platform 90. Laser 92 is then activated so laser beam 98 will scan

unconsolidated (e.g., liquid or powdered) material 86 disposed over surface 100 of platform 90 to at least partially consolidate (e.g., polymerize to at least a semisolid state) material 86 at selected locations, defining the boundaries of a first layer 122A of base support 122 and filling in solid portions thereof. Platform 90 is then lowered by a distance equal to the thickness of second layer 122B, and laser beam 98 scanned over selected regions of the surface of material 86 to define and fill in the second layer while simultaneously bonding the second layer to the first. The process may be ~~then~~ repeated, as often as necessary, layer by layer, until base support 122 is completed. Platform 90 is then moved relative to mirror 94 to form any additional base supports 122 on platform 90 or a substrate disposed thereon or to fabricate objects upon platform 90, base support 122, or a substrate, as provided in the control software. The number of layers required to erect support 122 or one or more other objects to be formed depends upon the height of the object or objects to be formed and the desired layer thicknesses of layers 20A, 20B, etc. The layers of a stereolithographically fabricated structure may have different thicknesses.

Please replace paragraph number **[0059]** with the following rewritten paragraph:

[0059] If a recoater blade 102 is employed, the process sequence is somewhat different. In this instance, surface 100 of platform 90 is lowered into unconsolidated (e.g., liquid) material 86 below surface level 88 a distance greater than a thickness of a single layer of material 86 to be cured, then raised above surface level 88 until platform 90, a substrate disposed thereon, or a structure being formed on platform 90 or a substrate thereon is precisely one layer's thickness below blade 102. Blade 102 then sweeps horizontally over platform 90 or (to save time) at least over a portion thereof on which one or more objects are to be fabricated to remove excess material 86 and leave a film of precisely the desired thickness. Platform 90 is then lowered so that the surface of the film and ~~material~~ surface level 88 are coplanar and the surface of the unconsolidated material 86 is still. Laser 92 is then initiated to scan with laser beam 98 and define the first layer 20A. The process is repeated, layer by layer, to define each succeeding layer and simultaneously bond same to the next lower layer until all of the layers of the object or objects to be fabricated are completed. A more detailed discussion of this sequence and

apparatus for performing same is disclosed in U.S. Patent 5,174,931, previously incorporated herein by reference.

Please replace paragraph number **[0063]** with the following rewritten paragraph:

[0063] In practicing the present invention, a commercially available stereolithography apparatus operating generally in the manner as that described above with respect to apparatus 80 of FIG. 11 may be employed, but with further additions and modifications as hereinafter described for practicing the method of the present invention. For example and not by way of limitation, the SLA-250/50HR, SLA-5000 and SLA-7000 stereolithography systems, each offered by 3D Systems, Inc., of Valencia, California, are suitable for modification. Photopolymers believed to be suitable for use in practicing the present invention include Cibatool SL 5170 and SL 5210 resins for the SLA-250/50HR system, Cibatool SL 5530 resin for the SLA-5000 and 7000 systems, and Cibatool SL 7510 resin for the SLA-7000 system. All of these photopolymers are available from Ciba Specialty Chemicals ~~Corporation.~~ Inc.

Please replace paragraph number **[0077]** with the following rewritten paragraph:

[0077] Referring now to both FIGs. 11 and 12, it should be noted that apparatus 80, 180 useful in the methods of the present invention include cameras 140 which are in communication with computers 82, 182, respectively, and are preferably located, as shown, in close proximity to optics and mirror 94 located above surface 100, 200 of support platform 90, 190. Each camera 140 may be any one of a number of commercially available cameras, such as ~~capacitive-coupled~~ capacitive-coupled discharge (CCD) cameras available from a number of vendors. Suitable circuitry as required for adapting the output of camera 140 for use by computer 82, 182 may be incorporated in a board 142 installed in computer 82, 182 which is programmed as known in the art to respond to images generated by camera 140 and processed by board 142. Camera 140 and board 142 may together comprise a so-called "machine vision system" and, specifically, a "pattern recognition system" (PRS), the operation of which will be described briefly below for a better understanding of the present invention. Alternatively, a self-contained

machine vision system available from a commercial vendor of such equipment may be employed. For example, and without limitation, such systems are available from Cognex Corporation of Natick, Massachusetts. For example, the apparatus of the Cognex BGA Inspection Package™ or the SMD Placement Guidance Package™ may be adapted to the present invention, although it is believed that the MVS-8000™ product family and the Checkpoint® product line, the latter employed in combination with Cognex PatMax™ software, may be especially suitable for use in the present invention.

Please replace paragraph number **[0080]** with the following rewritten paragraph:

[0080] One or more semiconductor devices 10, carrier substrates 30, or other semiconductor device components may be placed on surface 100, 200 of platform 90, 190 for fabrication of intermediate conductive elements 20 in communication with contact pads thereof (e.g., contact pads 12 of semiconductor device 10) (shown in FIGs. 1-4). One or more semiconductor devices 10, carrier substrates 30, or other semiconductor device components may be held on or supported above platform 90, 190 by stereolithographically formed base supports 122. When apparatus 80 is used, these base supports 122 are formed by sequentially disposing one or more layers of material 86 on surface 100 and selectively altering material 86 by use of laser 92. Apparatus 180 forms base supports 122 by selectively depositing one or more layers of material 186 from spray heads 192.

Please replace paragraph number **[0081]** with the following rewritten paragraph:

[0081] Camera 140 is then activated to locate the position and orientation of each semiconductor device 10, carrier substrate 30, or other type of semiconductor device component upon which intermediate conductive elements 20 are to be fabricated. The features of each semiconductor device 10, carrier substrate 30, or other type of semiconductor device component are compared with those in the data file residing in memory, the locational and orientational data for each semiconductor device 10, carrier substrate 30, or other type of semiconductor device component then also being stored in memory. It should be noted that the data file representing

the design size, shape and topography for each semiconductor device 10, carrier substrate 30, or other type of semiconductor device component may be used at this juncture to detect physically defective or damaged semiconductor devices 10, carrier substrates 30, or other types of semiconductor device components prior to fabricating intermediate conductive elements 20 thereon or before conducting further packaging of semiconductor devices 10, carrier substrates 30, or other types of semiconductor device components. Accordingly, such damaged or defective semiconductor devices 10, carrier substrates 30, or other types of semiconductor device components can be deleted from the process of fabricating intermediate conductive elements 20 and from further packaging. It should also be noted that data files for more than one type (size, thickness, configuration, surface topography) of each semiconductor device 10, carrier substrate 30, or other type of semiconductor device component may be placed in computer memory and computer 82, 182 programmed to recognize not only the locations and orientations of each semiconductor device 10, carrier substrate 30, or other type of semiconductor device component, but also the type of semiconductor component at each location upon platform 90, 190 so that material 86 may be at least partially consolidated by laser beam 98 or material 186 selectively deposited by spray heads 192 in the correct pattern and to the height required to define intermediate conductive elements 20 in the appropriate, desired locations on each semiconductor device 10, carrier substrate 30, or other semiconductor device component.

Please replace paragraph number **[0082]** with the following rewritten paragraph:

[0082] When apparatus 80 is used, as depicted in FIGs. 11 and 13, the one or more semiconductor devices 10, carrier substrates 30, or other semiconductor device components on platform 90 may then be submerged partially below the surface level 88 of unconsolidated (e.g. liquid) material 86 to a depth greater than the thickness of a first layer of material 86 to be at least partially consolidated (e.g., cured to at least a semisolid state) to form the lowest layer of each intermediate conductive element 20 at the appropriate location or locations on each semiconductor device 10, carrier substrate 30, or other type of semiconductor device component, then raised to a depth equal to the layer thickness, the surface level 88 of material 86 being

allowed to become calm. Photopolymers that are useful as material 86 exhibit a desirable dielectric constant and low shrinkage upon cure, are of sufficient (i.e., semiconductor grade) purity, exhibit good adherence to other semiconductor device materials, and have a coefficient of thermal expansion (CTE) similar to that of the materials adjacent thereto. Preferably, the CTE of material 86 is sufficiently similar to that of the adjacent materials to prevent undue stressing thereof during thermal cycling of semiconductor device 10, carrier substrate 30, or other semiconductor device component in testing, subsequent processing, and subsequent normal operation. Exemplary photopolymers exhibiting these properties are believed to include, but are not limited to, the above-referenced resins from Ciba Specialty ~~Chemical Company.~~ Chemicals Inc. One area of particular concern in determining resin suitability is the substantial absence of mobile ions and, specifically, fluorides.

Please replace paragraph number **[0083]** with the following rewritten paragraph:

[0083] Laser 92 is then activated and scanned to direct laser beam 98, under control of computer 82, toward specific locations of surface level 88 relative to each semiconductor device 10, carrier substrate 30, or other type of semiconductor device component to effect the aforementioned partial cure of material 86 to form a first layer 20A of each intermediate conductive element 20. Platform 90 is then lowered into reservoir 84 and raised a distance equal to the desired thickness of another layer 20B of each intermediate conductive element 20, and laser 92 is activated to add another layer 20B to each intermediate conductive element 20 under construction. This sequence continues, layer by layer, until each of the layers of intermediate conductive elements 20 has been completed.

Please replace paragraph number **[0087]** with the following rewritten paragraph:

[0087] Alternatively, intermediate conductive elements 20 or other stereolithographically fabricated structures may each be formed as a partially cured outer skin extending above active surface 14 of semiconductor device 10 or above surface 34 of carrier substrate 30 and forming a dam within which unconsolidated material 86 can be contained. This

may be particularly useful where intermediate conductive elements 20 or other structures protrude a relatively high distance above active surface 14. In this instance, support platform 90 may be submerged so that material 86 enters the area within the dam and raised above surface level 88, and then laser beam 98 activated and scanned to at least partially cure material 86 residing within the dam or, alternatively, to merely cure a ~~"skin" comprising a contact surface,~~ "skin," a final cure of the material of intermediate conductive elements 20 or other structures under construction being effected subsequently by broad-source UV radiation in a chamber, or by thermal cure in an oven. In this manner, intermediate conductive elements 20 and other structures of extremely precise dimensions may be formed of material 86 by apparatus 80 in minimal time.

Please replace paragraph number **[0088]** with the following rewritten paragraph:

[0088] Once intermediate conductive elements 20 or other structures, or at least the outer skins thereof, have been fabricated, platform 90 is elevated above surface level 88 of material 86 and platform 90 is removed from apparatus 80, along with semiconductor device 10, carrier substrate 30, or another semiconductor device component upon which intermediate conductive elements 20 or other structures have been stereolithographically fabricated. Excess, unconsolidated material 86 (e.g., excess uncured liquid) may be manually removed from platform 90, from any substrate disposed thereon, and from intermediate conductive elements 20 or other stereolithographically fabricated structures. Each semiconductor device 10, carrier substrate 30, or other semiconductor device component is removed from platform 90, such as by cutting the semiconductor device component free of base supports 122. Alternatively, base supports 122 may be configured to readily release semiconductor devices 10, carrier substrates 30, or other semiconductor device components. As another alternative, a solvent may be employed to release base supports 122 from platform 90. Such release and solvent materials are known in the art. See, for example, U.S. Patent No. 5,447,822 referenced above and previously incorporated herein by reference.

Please replace paragraph number **[0091]** with the following rewritten paragraph:

[0091] Referring again to FIGs. 12 and 13, when apparatus 180 is used to fabricate intermediate conductive elements 20, spray heads 192 direct liquified material 186 onto the appropriate location or locations of the one or more semiconductor devices 10, carrier substrates 30, or other semiconductor device components on platform 190, 90. The material is permitted to solidify to form the lowest layer 20A of each intermediate conductive element 20. Thermoplastic polymers that are useful as material 186 exhibit desirable electrical conductivity, exhibit low shrinkage upon solidification, substantially maintain their structural integrity under normal operating conditions (e.g., operating temperatures of the semiconductor device), are of sufficient (i.e., semiconductor grade) purity, exhibit good adherence to other semiconductor device materials, and have a coefficient of thermal expansion (CTE) similar to that of the materials adjacent thereto. Preferably, the CTE of material 186 is sufficiently similar to that of the adjacent materials to prevent undue stressing thereof during thermal cycling of semiconductor device 10, carrier substrate 30, or another semiconductor device component in testing, subsequent processing, and subsequent normal operation.

Please replace paragraph number **[0094]** with the following rewritten paragraph:

[0094] Once intermediate conductive elements 20 or other structures have been fabricated, platform 190 is removed from apparatus 180, along with semiconductor device 10, carrier substrate 30, or another semiconductor device component upon which intermediate conductive elements 20 or other structures have been stereolithographically fabricated. Each semiconductor device 10, carrier substrate 30, or other semiconductor device component is removed from platform 190, such as by cutting the semiconductor device component free of base supports 122. Alternatively, base supports 122 may be configured to readily release semiconductor devices 10, carrier substrates 30, or other semiconductor device components. As another alternative, a solvent may be employed to release base supports 122 from platform 190. Such release and solvent materials are known in the art. See, for example, U.S. Patent No. 5,447,822 referenced above and previously incorporated herein by reference.

Please replace paragraph number **[0096]** with the following rewritten paragraph:

[0096] The use of a stereolithographic process as exemplified above to fabricate intermediate conductive elements 20 is particularly advantageous since a large number of intermediate conductive elements 20 may be substantially simultaneously fabricated in a short time, the positioning thereof is computer controlled and extremely precise, wastage of material is minimal, and the stereolithography method requires minimal handling of semiconductor devices 10, carrier substrates 30, or other semiconductor device components.

Please replace paragraph number **[0097]** with the following rewritten paragraph:

[0097] Stereolithography is also an advantageous method of fabricating intermediate conductive elements 20 according to the present invention since stereolithography can be conducted at temperatures that will not damage or induce significant thermal stress on the semiconductor device components during fabrication of intermediate conductive elements 20 thereon. The stereolithography fabrication process may also be used to simultaneously form intermediate conductive ~~structures~~ elements 20 on several semiconductor device components or assemblies, saving fabrication time and expense. As the stereolithography method of the present invention recognizes specific semiconductor devices 10, carrier substrates 30, and other semiconductor device components, variations between different semiconductor device components are accommodated. Accordingly, when the stereolithography method of the present invention is employed, intermediate conductive elements 20 can be simultaneously fabricated on different types of semiconductor device components or assemblies of semiconductor device components.

Please replace paragraph number **[00100]** with the following rewritten paragraph:

[00100] Each intermediate conductive element 20 is substantially entirely carried along the length thereof upon either semiconductor device 10 or carrier substrate 30. As illustrated in FIG. 2, each intermediate conductive element 20 extends across a portion of active surface 14 of semiconductor device 10, down a lateral edge 18 of semiconductor device 10, and across a

portion of surface 34 of carrier substrate 30. A first end 22 of each intermediate conductive element 20 is in contact with a bond pad 12 and a second end 24 of intermediate conductive element 20 is connected to a contact pad 32 of carrier ~~substrate 32~~ substrate 30.

Please replace paragraph number **[00103]** with the following rewritten paragraph:

[00103] With continued reference to FIGs. 3 and 4, substantially the entire lengths of intermediate conductive elements 20 are carried by semiconductor devices 10, 10′. As illustrated in FIG. 4, each intermediate conductive element 20 extends across a portion of active surface 14 of a first semiconductor device 10, over an interface 17 between abutting lateral edges 18, 18′ of the two semiconductor devices 10, 10′, and across a portion of active surface 14′ of the second semiconductor device 10′. A first end 22 of each intermediate conductive ~~structure~~ element 20 is in contact with a bond pad 12 of one semiconductor device 10 and a second end 24 of intermediate conductive ~~structure~~ element 20 is connected to a bond pad 12′ of the other semiconductor device 10′ (FIG. 3).

Please replace paragraph number **[00107]** with the following rewritten paragraph:

[00107] When both intermediate conductive elements 20′ and substrate layer 31 are stereolithographically fabricated, carrier substrates 30 that carry intermediate conductive elements 20′ on both surfaces thereof may be fabricated by forming a first, bottom set of intermediate conductive elements 20′ on a platform of a suitable stereolithography apparatus, forming substrate layer 31 over the first set of intermediate conductive ~~traces~~ elements 20′, then forming a second, upper set of intermediate conductive elements 20′ on substrate layer 31. Any vias 36 that extend vertically through substrate layer 31 may be fabricated before, during, or after the fabrication of substrate layer 31. When both intermediate conductive elements 20′ and substrate layer 31 are fabricated by use of stereolithography, the same stereolithographic technique and apparatus are preferably employed to fabricate intermediate conductive elements 20′ and substrate layer 31. Accordingly, carrier substrate 30 need not be moved between different stereolithographic apparatus during fabrication thereof. However, the use of

different stereolithographic techniques and apparatus to fabricate intermediate conductive elements 20′ and substrate layer 31 are also within the scope of the present invention.

Please replace paragraph number **[00111]** with the following rewritten paragraph:

[00111] When both intermediate conductive elements 20′ and substrate layer 31′ are stereolithographically fabricated, a first, bottom set of intermediate conductive elements 20′ may be formed on a platform of a suitable stereolithography apparatus, forming a first substrate layer 31′ over or laterally adjacent to the first set of intermediate conductive elements 20′. The appropriate sequence of forming intermediate conductive elements 20′ and substrate layers 31′ then continues until a multilayer carrier substrate 30′ of desired configuration has been fabricated. Any vias 36 that extend vertically through one or more substrate layers 31′ may be fabricated before, during, or after the fabrication of the substrate layers 31′. When both intermediate conductive elements 20′ and substrate layers 31′ are fabricated by use of stereolithography, the same stereolithographic technique and apparatus are preferably employed to fabricate intermediate conductive elements 20′ and substrate layers 31′. Accordingly, carrier substrate 30′ need not be moved between different stereolithographic apparatus during fabrication thereof. However, the use of different stereolithographic techniques and apparatus to fabricate intermediate conductive elements 20′ and substrate layers 31′ are also within the scope of the present invention.